

MC10EP33

÷ 4 Divider

The MC10EP33 is an integrated ÷ 4 divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. If used, the V_{BB} output should be bypassed to ground with a 0.01 μ F capacitor.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EP33's in a system.

- 320ps Propagation Delay
- 3 GHz Typical Toggle Frequency
- PECL mode: 3.0V to 5.5V V_{CC} with $V_{EE} = 0V$
- ECL mode: 0V V_{CC} with $V_{EE} = -3.0V$ to $-5.5V$
- Internal Input Resistors: Pulldown on D, \overline{D}
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 91 devices

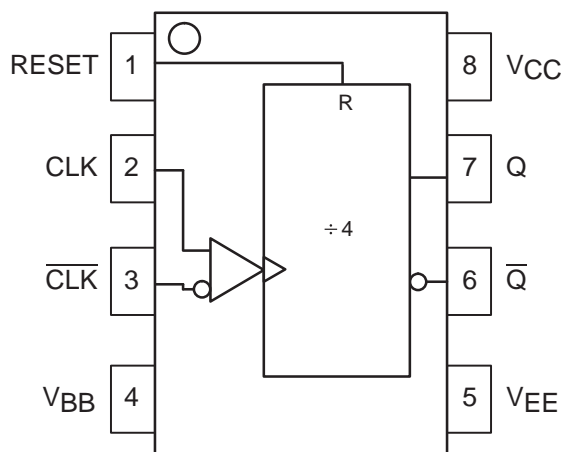


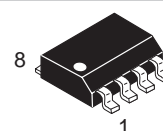
Figure 1. 8-Lead Pinout (Top View) and Logic Diagram



ON Semiconductor

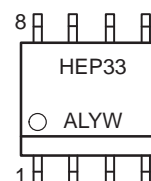
Formerly a Division of Motorola

<http://onsemi.com>



**SO-8
D SUFFIX
CASE 751**

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION

PIN	FUNCTION
CLK, \overline{CLK}	ECL Clock Inputs
Reset	ECL Asynchronous Reset
V_{BB}	Reference Voltage Output
Q, \overline{Q}	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

TRUTH TABLE

CLK	\overline{CLK}	RESET	Q	\overline{Q}
X	X	Z	L	H
Z	\overline{Z}	L	F	F

Z = LOW to HIGH Transition
 \overline{Z} = HIGH to LOW Transition
 F = Divide by 4 Function

ORDERING INFORMATION

Device	Package	Shipping
MC10EP33D	SOIC	98 Units/Rail
MC10EP33DR2	SOIC	2500 Tape & Reel

MC10EP33

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply ($V_{CC} = 0V$)	-6.0 to 0	VDC
V_{CC}	Power Supply ($V_{EE} = 0V$)	6.0 to 0	VDC
V_I	Input Voltage ($V_{CC} = 0V$, V_I not more negative than V_{EE})	-6.0 to 0	VDC
V_I	Input Voltage ($V_{EE} = 0V$, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	41 to 44 $\pm 5\%$	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

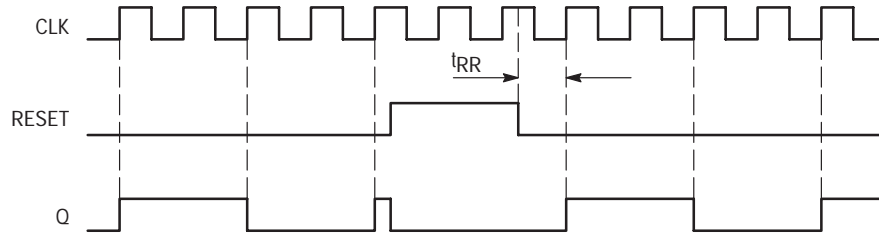


Figure 2. Timing Diagram

MC10EP33

DC CHARACTERISTICS, ECL/LVECL ($V_{CC} = 0V$; $V_{EE} = -5.5V$ to $-3.0V$) (Note 4.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	18	26	34	18	26	34	18	26	34	mA
VOH	Output HIGH Voltage (Note 2.)	-1135	-1060	-885	-1070	-945	-820	-1010	-885	-760	mV
VOL	Output LOW Voltage (Note 2.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
VIH	Input HIGH Voltage Single Ended	-1210		-885	-1145		-820	-1085		-760	mV
VIL	Input LOW Voltage Single Ended	-1935		-1610	-1870		-1545	-1810		-1485	mV
VBB	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 3.)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. $V_{CC} = 0V$, $V_{EE} = V_{EEmin}$ to V_{EEmax} , all other pins floating.

2. All loading with 50 ohms to $V_{CC}-2.0$ volts.

3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

4. Input and output parameters vary 1:1 with V_{CC} .

DC CHARACTERISTICS, LVPECL ($V_{CC} = 3.3V \pm 0.3V$, $V_{EE} = 0V$) (Note 8.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	18	26	34	18	26	34	18	26	34	mA
VOH	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
VOL	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
VIH	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
VIL	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
VBB	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. $V_{CC} = 3.3V$, $V_{EE} = 0V$, all other pins floating.

6. All loading with 50 ohms to $V_{CC}-2.0$ volts.

7. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

8. Input and output parameters vary 1:1 with V_{CC} .

MC10EP33

DC CHARACTERISTICS, PECL ($V_{CC} = 5.0V \pm 0.5V$, $V_{EE} = 0V$) (Note 12.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	18	26	34	18	26	34	18	26	34	mA
VOH	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
VOL	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
VIH	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
VIL	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
VBB	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. $V_{CC} = 5.0V$, $V_{EE} = 0V$, all other pins floating.

10. All loading with 50 ohms to $V_{CC} - 2.0$ volts.

11. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

12. Input and output parameters vary 1:1 with V_{CC} .

AC CHARACTERISTICS ($V_{CC} = 0V$; $V_{EE} = -3.0V$ to $-5.5V$) or ($V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{max}	Maximum Toggle Frequency (Note 13.)	2.5	3.0		2.5	3.0		2.5	3.0		GHz
t _{PLH} , t _{PHL}	Propagation Delay to Output Differential CLK/Q RESET/Q	225 200	300 270	360 360	250 250	320 320	380 380	275 275	350 350	425 425	ps
t _{RR}	Set/Reset Recovery	300	225		300	225		300	225		ps
t _{SKEW}	Duty Cycle Skew (Note 14.)		5.0	20		5.0	20		5.0	20	ps
t _{PW}	Minimum Pulse Width RESET	550	480		550	480		550	480		ps
t _{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V _{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t _r t _f	Output Rise/Fall Times Q, \bar{Q} (20% – 80%)	90	170	200	100	180	250	120	200	280	ps

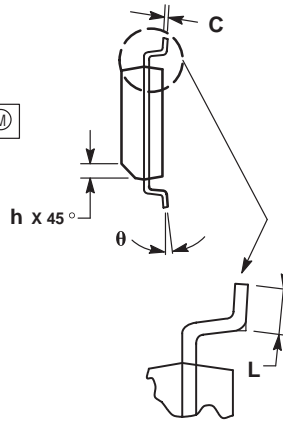
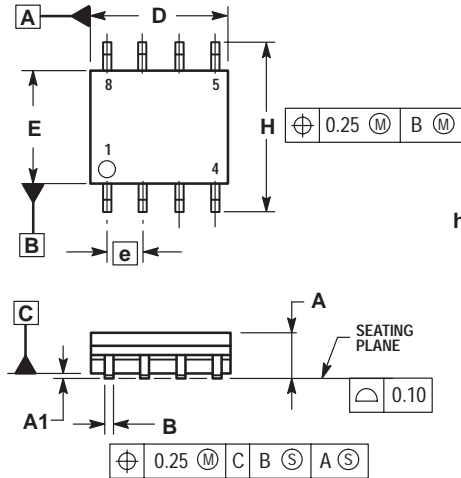
13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

14. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP33

PACKAGE DIMENSIONS

SO-8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-06
ISSUE T




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

Notes

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

USA/EUROPE Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

Fax Response Line*: 303-675-2167
800-344-3810 Toll Free USA/Canada
*To receive a Fax of our publications

N. America Technical Support: 800-282-9855 Toll Free USA/Canada

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549

Phone: 81-3-5487-8345
Email: r14153@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.